IN THE DRAWINGS

The attached sheet of drawings includes changes to Fig. 6. This sheet, which includes Fig. 6, replaces the original sheet including Fig. 6.

Attachment: Replacement Sheet

REMARKS/ARGUMENTS

Favorable reconsideration of this application is respectfully requested.

The specification is amended by the present response to correct minor informalities therein.

A replacement Figure 6 is also submitted that properly labels element 20.

The changes made to the specification and in replacement Figure 6 are deemed to be self-evident from the original disclosure, and thus are not deemed to raise any issues of new matter.

The claims are also amended by the present response to address the objections noted on pages 2-3 of the Office Action.

Claims 1-8 are pending in this application. Claim 6 was rejected under 35 U.S.C. § 112, second paragraph. Claims 1-8 were rejected under 35 U.S.C. § 103(a) as unpatentable over applicants' admitted art as evidenced by U.S. patent 6,728,901 to Rajski et al. (herein "Rajski"), U.S. patent 4,811,345 to Johnson, U.S. patent 3,872,245 to Sagawa et al. (herein "Sagawa"), U.S. patent 3,623,020 to Mao, and U.S. patent 4,188,665 to Nagel et al. (herein "Nagel").

Addressing first the rejection of claim 6 under 35 U.S.C. § 112, second paragraph, that rejection is traversed by the present response.

Claim 6 is believed to be proper. As shown for example in Figure 3 in the present specification the serial-to-parallel converter 15 receives three different inputs, but only converts the input from a scanning output terminal 26 to parallel data. The serial-to-parallel converter 15 has two other inputs from a clock output terminal 11 and an enable-signal output terminal 13, but only the signal from the scanning output terminal 26 is converted into parallel data. That subject matter is discussed for example in the present specification at page 9, lines 1-14. Thus, claim 6 is believed to be proper as written.

Addressing now the rejection of claims 1-8 under 35 U.S.C. § 103(a), that rejection is traversed by the present response.

The outstanding Office Action points out several features in the claims that are not disclosed in the admitted art, but then appears to indicate the admitted art only needs a teaching of a linear feedback shift register (LFSR) to fully meet the claim limitations.

In reply to that basis for the rejection, applicants first note the outstanding Office Action has not at all indicated how the noted secondary art is being combined with the disclosure in the admitted art to fully meet all the claim limitations. No specific disclosures in the secondary cited references are specifically being applied against the claims, and is unclear on what basis each of the secondary cited references to Rajski, Johnson, Sagawa, Mao, and Nagel are being utilized and combined with the disclosure in the admitted art. Clearly the Office Action has not indicated how each element recognized as not disclosed in the admitted art is disclosed in the applied secondary art and is properly combinable with the admitted art. Therefore, any maintained rejection is requested to be clearly explained under a proper obviousness rejection.

Moreover, applicants respectfully submit the outstanding rejection is not fully considering each of the claimed features and the differences between the claims and the admitted art of Figure 6.

Independent claim 1 positively recites a "feed-back signal line through which a signal from the scanning output terminal of the last-stage scanning F/F circuit is fed back", "at least one data selector to select either an external scanning line or the signal fed back from the last-stage scanning F/F circuit" and for supplying a selected signal to the "first-stage scanning F/F circuit", "at least one scanning controller to supply a control signal to the data selector" and for controlling an operational state of a desired-stage scanning F/F circuit, and "an external

scanning output terminal" for detecting and externally outputting the output signal of the last-stage scanning F/F circuit from the logic circuit.

With the above-noted claimed features a scanning test circuit (flip-flop F/F) is provided with any of the logic circuits, and the scanning test can be performed in an arbitrary logic circuit. The flip-flop stores the state of the logic circuit at executing the test.

In a scanning test mode, and with reference to Figures 1-5 in the present specification as a non-limiting example, the data selector 3 executes the scanning test according to a predetermined bit pattern input, and outputs the result through SOUT of the flip-flops. Since the result is a predetermined bit string, the result is externally obtained by a serial-parallel conversion.

Moreover, according to advantages possible by the claimed invention, at debugging an arbitrary logic circuit, there is a case in which the state of the logic circuit at an error occurrence, for example, is required to be output to an external device. To meet such a requirement, a logic circuit may stop its operation, and the data selector 3 can be set to a feedback mode. Since the flip-flop circuits store the state of the logic circuit, when the clocks of the stage-number of the flip-flop are input, the state of the desired stage flip-flop is output through SOUT to the external device.

Thereby, with the claimed features it is possible to externally detect an internal state of the logic circuit by using a scanning test circuit that is provided with the logic circuit.

The background scanning F/F circuit shown in Figure 6 in the present specification does not include any of the claimed "feed-back signal line", "at least one data selector", "at least one scanning controller", and "external scanning output terminal".

The only articulated basis for modifying the admitted art of Figure 6 to meet the claim limitations appears to be that Rajski discloses a linear feed-back shift register (LFSR). However, even if that element corresponds to the claimed "feed-back line", which applicants

dispute, no disclosure in Rajski fully discloses each of the above-noted "at least one data selector", "at least one scanning controller", and "external scanning output terminal". Thereby, no teachings in Rajski fully cure the recognized deficiencies in the admitted art of Figure 6. Further, no teachings in any of the further cited references to Johnson, Sagawa, Mao, or Nagel were even cited to actually disclose features to cure the recognized deficiencies in the admitted art of Figure 6.

Moreover, applicants respectfully submit the basis for the outstanding rejection is even misconstruing the teachings in Rajski relative to the claimed features.

Rajski discloses an apparatus and method provided for an arithmetic built-in self-test (ABIST) of a number of peripheral devices having parallel scan registers coupled to a processor core, all within an integrated circuit, and operating logic that generates test patterns for the peripheral devices using the data paths to the processor core, loads the test patterns into the parallel scan registers of the peripheral devices, recovers test responses from the parallel scan registers, and compacts responses from the parallel devices once again using the data paths of the processor core.[1]

Rajski discloses feedback paths for recovering a response from a parallel scan register. However, Rajski clearly differs from the claims in that Rajski does not disclose or suggest:

> at least one data selector to select either an external scanning signal or the signal fed back from the last-stage scanning F/F circuit, the selected signal being supplied to the scanning input terminal of the first-stage scanning F/F circuit;
>
> at least one scanning controller to supply a control signal to the data selector so that the signal fed back from the last-stage scanning F/F circuit is supplied to the scanning input terminal of the first-stage F/F scanning circuit, thus controlling each scanning F/F circuit in an internal scanning mode; and

[1] See the Abstract of Rajski.

an external scanning output terminal via which the signal fed back from the last-stage scanning F/F circuit is output from the logic circuit.

Even the basis for the outstanding rejection appears to only rely on Rajski to disclose a linear feedback shift register, but in that respect Rajski does not disclose any of the above-noted "at least one data selector", "at least one scanning controller", and "external scanning output terminal".

Moreover, Rajski merely performs a repetition of random data and its responses. Rajski does not detect an internal state of a logic circuit by outputting a signal through a scan output terminal, as possible by the device recited in independent Claim 1. In that way, the claimed subject matter differs significantly from the technology in Rajski.

In view of these foregoing comments, applicants respectfully submit clearly Rajski does not cure all the recognized deficiencies in the admitted art of Figure 6.

Moreover, and as noted above, no teachings in Johnson, Sagawa, Mao, or Nagel were even noted in the Office Action as to how they could be combined with the admitted art of Figure 6 to fully meet all the claim limitations. In that respect applicants also submit Johnson, Sagawa, Mao, and Nagel do not provide any disclosure that would cure all the recognized deficiencies in the admitted art of Figure 6.

In view of the present response, applicants respectfully submit clearly the claims as written distinguish over the applied art.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

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